

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SANG Y. LEE, VASANT B. RAO, JEFFREY SOREFF,
JAMES WARNOCK, and DAVID WINSTON

Appeal 2008-004895
Application 10/897,347
Technology Center 2100

Decided:¹ July 1, 2009

Before ST. JOHN COURTENAY III, THU A. DANG, and STEPHEN C.
SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON APPEAL

¹ The two month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

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STATEMENT OF THE CASE

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-3, 6-9, 11, and 15-24. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Invention

The invention relates generally to circuit simulation and, more particularly, to simulation of non-leading edge transitions (Spec. 1, ll. 3-5).

Independent claim 1 is illustrative:

1. A computer system for determining whether a pulse is wide enough to serve as a clock to a latch, the computer system comprising:

a memory;

a circuit simulated in the memory; and

a processor coupled to the memory,

wherein the circuit simulated in the memory comprises a clock chopper block and a latch, wherein the clock chopper block provides a clock input to the latch;

wherein the clock chopper block comprises an inverter and a NOR gate, wherein the inverter receives a first signal as an input and provides a second signal as an output, wherein the NOR gate receives the first signal and second signal as inputs and provides a third signal as an output, and wherein the third signal is provided as the clock input to the latch;

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wherein a falling transition of the first signal causes a rising transition of the third signal after a first delay and wherein the falling transition of the first signal causes a rising transition of the second signal that causes a falling transition of the third signal after a second delay;

wherein the processor is programmed to capture, responsive to the falling transition of the first signal, the rising transition of the third signal and the falling transition of the third signal;

wherein the processor is programmed to determine the first delay and the second delay;

wherein the processor is programmed to determine a pulse width of the third signal based on the first delay and the second delay; and

wherein the processor is programmed to determine whether the pulse width of the third signal is wide enough to serve as the clock input to the latch.

References

The Examiner relies upon the following references as evidence in support of the rejections:

Chung	US 4,808,840	Feb. 28, 1989
Fusco	US 6,067,652	May 23, 2000
Rahmat	US 6,567,773 B1	May 20, 2003

Rejection

Claims 1-3, 8, 9, 11, 15, 16, 19-21, and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Fusco and Chung.

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Claims 6, 7, 17, 18, 22, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Fusco, Chung, and Rahmat.

ISSUE

Appellants argue that combining the teachings of Fusco and Chung to determine whether a pulse width of a signal is wide enough to serve as the clock input to a latch “would require an inventive leap or prior knowledge of the present invention” (App. Br. 8).

Issue: Have Appellants shown that the Examiner erred by relying upon impermissible hindsight in combining the Fusco and Chung references to determine whether a pulse width of a signal is wide enough to serve as the clock input to a latch?

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

1. Chung “relates to apparatus and method [*sic*] for decreasing the setup time of an edge-triggered latch, as well as the probability of its having a metastability problem” (col. 1, ll. 7-10).
2. Chung teaches “[t]he gates of both T₄ and T₃ are controlled by a clock ϕ' which is a time delayed pulse of ϕ . One method of generating ϕ' is by delaying the rising edge (the triggering edge) of clock ϕ . A circuit for accomplishing such purpose is [the clock chopper block] illustrated in FIG. 2” (col. 2, ll. 45-49).

3. Fusco teaches that “[t]o produce an [integrated circuit], a manufacturer must first design an electronic circuit to integrate (i.e., manufacture) into a chip. This stage of the design process typically requires a designer to simulate a circuit description in a circuit simulator and compare the simulated results with expected results to verify the proper operation of the circuit design” (col. 1, ll. 15-21).

PRINCIPLES OF LAW

Obviousness

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

“A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning.” *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 421 (2007).

ANALYSIS

The Examiner has found that one of ordinary skill in the art would have reason to combine the teachings of Fusco and Chung because “Chung expressly teaches the advantages of the circuit . . . while Fusco expressly teaches the advantages of circuit simulation” (Ans. 5). Such general reasoning bears close analysis.

Chung “relates to apparatus and method [*sic*] for decreasing the setup time of an edge-triggered latch, as well as the probability of its having a metastability problem” (FF 1). Appellants stipulate that Chung “does appear to teach a clock chopper block that is used as a clock input” (App. Br. 7). But Chung discloses the clock chopper block merely as an example of how to create a time delayed pulse for controlling two gates within the edge-triggered latch taught by Chung (FF 2). Absent is any teaching or suggestion of the pulse circuitry testing the edge-triggered latch’s efficacy given a particular pulse width.

Fusco teaches that during an electronic circuit’s design phase, a designer typically must “simulate a circuit description in a circuit simulator and compare the simulated results with expected results to verify the proper operation of the circuit design” (FF 3). However, Fusco does not discuss the simulation of latches, either with or without a clock chopper block input. Nor does Fusco provide data capture and analysis teachings particular to such simulations.

To combine Fusco and Chung in the manner suggested by the Examiner, an artisan would have to use the clock chopper block of Chung for the purpose of generating a test clock pulse as part of a latch circuit simulation. The Examiner does not find that the disclosure of Fusco or the clock chopper block of Chung is specifically directed to latch testing. Based upon our review of the evidence before us, it is our view that neither reference contains sufficient teachings or suggestions such that one of ordinary skill in the art would have reasonably looked to the other to form

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the combination proffered by the Examiner. Moreover, the Examiner has failed to respond to Appellants' allegation of hindsight, having only responded to Appellants' arguments to the extent that they "appear to be directed to the references' alleged failure to teach the [invention's] claimed steps" (Ans. 10).

Therefore, we are unconvinced that even an artisan possessing creativity and common sense, and having knowledge of latches and circuit simulation software, would have reasonably combined Fusco and Chung in the manner suggested by the Examiner, *but for* having the benefit of the instant claims to impermissibly use as a guide. Accordingly, we find Appellants have met their burden of showing the Examiner erred in rejecting independent claim 1, and of claims 2, 3, 6-9, 11, and 15-24, which fall therewith.

CONCLUSION

Based on the findings of facts and analysis above, we find Appellants have demonstrated the Examiner erred by relying upon impermissible hindsight in combining the Fusco and Chung references.

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DECISION

We reverse the Examiner's decision rejecting claims 1-3, 6-9, 11, and
15-24.

REVERSED

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